Feature level test patterns for characterizing residual process effects

Andrew R. Neureuther, Greg McIntyre, Frank Gennari, and Michael Lam, Jason Cain, Garth Robins, Edward Huang, Jihong Choi, Ling Wang, Lei Yuan, Hideaki Oshima (Electronics Research Labs, EECS Department, Univ. of Calif., Berkeley, CA 94720, neureuth@eecs.berkeley.edu)

ABSTRACT

Layout test patterns are being pursued that are more sensitive than circuit patterns in detecting and quantifying residual processing effects. These patterns permit the rapid searching of layouts for the locations of worst-case process impacts, and may facilitate layout compensation at OPC speeds. These patterns have been taped-out along with snippets of circuits in preparation for experimental verification of the ability to link residual process effects to electronic design. The collection includes pattern-and-probe-based targets for measuring aberrations, illumination non-uniformity and etch-depth errors in phase-shifting masks, plasma etching with loading effects related to area and perimeter factors, and patterns for CMP orientation and feature proximity. The goal is to use these test patterns to develop maximum lateral impact functions for each individual process effect for use in fast-CAD techniques capable of inspecting large layouts.

Keywords: DFM, OPC, PPC, pattern matching, aberrations, fast-CAD, process robustness advisor

1. INTRODUCTION

A challenge in manufacturing is to give the circuit designer a nearly free hand during design and yet assure that every feature prints/transfers to size. Design rules cover the important basics but there are local lateral effects among features such as those due to aberrations and process proximity effects that are not accurately or efficiently described by design rules. This, for example, may be due to the large variety of layout geometries that might fall into their radius of interaction. An alternative approach to capturing these residual process effects in Design For Manufacturability (DFM) is to provide the circuit designer with a process robustness advisor that can be invoked at convenient times during the circuit layout process. While full rigorous process simulation might be possible, it is much more appropriate to develop fast-CAD methods that can process a layout block in its entirety to identify worst-case layout locations from a manufacturing perspective. An exploratory pattern-matching strategy has been implemented in a prototype system[1]. It is based on first identifying the surrounding pattern that would cause the maximum lateral impact from a physical process and then utilizing matching of that pattern to the layout to evaluate the degree of similarity of each point in the layout with the maximum lateral impact function.

This paper describes a recent tape-out of a set of test patterns designed to screen for residual effects over a variety of processes. The goal of the patterns and their use in processing is twofold. They will be used initially to scope out the level of severity and the lateral range of processing effects in lithography, etching and CMP. They and their derivatives will become maximum lateral impact functions for testing the predictability of the pattern matching approach. The mask design was undertaken in a collaborative industry and State of California project on Feature Level Compensation and Control. It is a multi-student test mask that includes test patterns from students on other projects as well.

This paper begins with a discussion of the opportunities of linking process to electronic design in Section 2, followed by the extraction of characteristics that have helped to make fast-CAD possible for predicting the effects of aberrations in Section 3. The full mask view and floor plan is presented in Section 4, which is followed by the details of various test patterns in Section 5.

2. LINKING PROCESS AND ELECTRONIC DESIGN

An important new opportunity in Design For Manufacturability is to link the pattern dependent nature of residual process proximity effects to the circuit design process. The optical proximity effects due to the lateral spillover of light among features induced by the low pass filtering of the lens is well known and accounted for in commercial Optical proximity Correction (OPC) treatments of layouts. An additional optical spillover among features occurs due to lens aberrations.

Design and Process Integration for Microelectronic Manufacturing II, edited by
Lars W. Liebmann, Proc. of SPIE Vol. 5379 (SPIE, Bellingham, WA, 2004)
0277-786X/04/$15 · doi: 10.1117/12.540685

Even for good lenses with Strehl ratios of 0.975, additional automatic compensation in Aberration Proximity Correction (APC) is likely necessary[2]. While less understood, plasma etching, CMP, etc. have proximity effects at a broader range of scales and merit Process Proximity Correction (PPC)[3,4].

There are of course many ways of linking to design other than through post-processing the geometry once the design layout has been finalized. A relatively unexplored approach is the development of a process robustness advisor that inspects the layout during circuit design. We have been making a prototype investigation of this class of CAD tool both for aberration effects[2] and for more general process effects in a 'No-Fault Assurance' approach[1]. The ability to generalize from aberrations to a broader set of residual effects is quite uncertain, hence the effort in this paper to develop test patterns to identify and characterize lateral, pattern-dependent effects in various types of processes.

3. LEARNING FROM FAST-CAD FOR ABERRATIONS

We begin by considering the general characteristics of process effects that will make them amenable to fast-CAD techniques for visualizing and possibly compensating for residual process effects. Many of the same characteristics could be exploited in fast methods for Process Proximity Correction. The characteristics that we list here are derived from our previous experience in using pattern matching for identifying and quantifying line-edge position shifts due to lens aberrations.

1. First it must be determined that lateral spillover is important for a process. In the case of aberrations, image simulation indicated that the presence of 0.025 waves RMS of individual odd aberrations as found in today's good lenses produced an amount of line-edge position shift that cannot be ignored. In the case of coma and higher order coma and by implication their combination, this shift was found to be about half as large as is being corrected by OPC.

2. It is necessary to find a maximal lateral impact function that describes the worst-case impact. In the case of small aberrations, this function is the Fourier transform of the optical path difference (OPD) function of the lens. The effect of the illumination can also be included by weighting each point in the pattern by its mutual coherence function.

3. It is required that the amount of spillover be relatable to the degree of similarity of the actual pattern with the maximum lateral impact function. In the case of aberrations, the spillover from signals coming through adjacent openings is naturally an addition or superposition of weighted positional contributions.

4. It is necessary to relate the amount of spillover to the change in a physical characteristic of the central feature. In the case of optical imaging, the impact of additional electric field spilled over onto the feature can be viewed as perturbing the image intensity and hence for odd-aberrations the line-edge position.

5. It is required that the detail in the layout and the detail in the maximum lateral impact function permit rapid computation. In the case of aberrations, the detail in the maximum lateral impact function is similar to a $k_1 = 0.5$ feature so that the layout and pattern length scales are compatible and neither pattern nor layout requires rescaling. In addition, it is important to choose the proper radius of influence of the pattern to be large enough to capture the influence range of the processing effect yet small enough to avoid excessive computation during the matching process.

Figure 2 illustrates the use of pattern matching for aberrations. Figure 2a shows a close-up of a mask location for a point at which the integrated match factor or pattern similarity is 0.374. Evaluating this match factor using a simple convolution approach is time consuming and can be accelerated 100 fold by pre-integrating techniques that compose integration over arbitrary rectangles from lookup tables for integration over semi-infinite quadrants. Figure 2b shows the largest match factor locations on a 417mm^2 mask layout with 36 million shapes and 2.6 billion test points. With pattern pre-integration, this mask could be processed in only 34 minutes on a 1 GHz desktop.

The resulting image intensity change and line-edge shift can be evaluated from the match factor using an image perturbation model. For verification purposes, the pattern-matcher has the capability to also extract the layout local to a

match point and link to SPLAT for rigorous aerial image simulation. The correlation of the match factor with the electric field change from rigorous SPLAT simulation is shown in Figure 3. The result is a highly correlated linear relationship suggesting that this process robustness advisor is giving good advice. In fact, the unphysical spread for negative match factors also provided good advice for the development of SPLAT as it revealed an incorrect symmetry speedup assumption buried in SPLAT that has since been fixed.

4. MASK FLOOR PLAN

The full layout of the multi-student process-EDA test mask is shown in Figure 4. This picture, and the other figures in this paper, was generated with the GDS Viewer for Windows PCs written by Frank Gennari[5]. The main field size is 105 x 105 mm. The targets are designed for 5X at a NA of 0.5 and for 4X at NA's of 0.63, 0.7 and 0.8. This mask has four phases: 0-, 90-, 180-, and 270-degrees. The large open areas are associated with CMP test structures. The mid-sized rectangular areas are filled in various manners to test for flare effects. The small line-like regions in the dark field areas contain the aberration, illumination and PSM self-test structures.

The floor plan is shown in Figure 5. The aberration monitors (A1) and metrology (MA) for a scanner are in a horizontal band across the middle of the mask. The aberration monitor for a stepper (A2) and metrology for a stepper (MB) are added on the diagonals. The illumination targets (I) use a mixture. The PSM self-monitor (P) is at several locations including one with a surround for adding to the effects of flare. The resist double-exposure test pattern (R) is in the middle of the mask. The plasma etch pattern has sizeable surrounding regions and thus only 5 locations. CMP is expected to have the longest-range effects and hence the most real estate and the fewest locations (C1, C2).

5. TEST PATTERNS

An example of a pattern and probe aberration monitor is shown in Figure 6. This target has 3-fold rotational symmetry and is for trifoil. The small openings to the right are isolated probes for calibration. The rings in the target spill light over onto the center when trifoil is present, thus making the probe intensity increase or decrease. By measuring the dose required to print the center probe relative to either the dose to clear or the dose to size, both the sign and amount of trifoil can be determined.[6]

Examples of two illumination monitors are shown in Figure 7. The linear phase grating, a four-phase chromeless mask pattern designed to diffract light into only the +1 and higher orders, is shown in Figure 7a. The projection lens pupil serves to clip only a particular portion of the illuminator, depending on the grating period and orientation. Multiple LPGs, arranged strategically on the mask, serve to capture various portions of the illuminator within the pupil. This allows for characterization of the illumination pupil-fill distribution as the dose each grating prints in resist is related to the total intensity captured within the pupil.[7]

Figure 7a shows an example of the linear phase ring, a four-phase mask pattern that is also designed to characterize tool illumination, but is based on the coherent proximity effect spillover of a surrounding pattern on a central position. This monitor, consisting of an Airy pattern multiplied by a linear phase progression corresponding to a particular illumination pupil position, serves to spill light coherently into the center position for only illumination from that designed target location.[8]

A test structure for monitoring the etch-depth of phased contact-sized regions is shown in Figure 8. This pattern, the interferometric-probe monitor for PSM performance, is also based on the proximity effect. It is designed to coherently spill electric field into the center of the pattern if either a phase and/or transmission imbalance exists between the phase regions. Due to the orthogonality of phase and transmission errors, a sub-printable interferometric probe of either 0 or 90-degree phase allows amplification and detection of either type of error. Sensitivity of the monitor is related to the pattern size and can theoretically achieve up to 1% of the clear field per degree phase error with a five-ring design (radius = 3.1 λ/NA).[9]

The SEMs in Figure 9 shows that the mask fabrication was of high quality even for these very challenging structures. AFM measurements show the desired profiles and are quite accurate in phase depth, even for small features. The phase-shifted contacts are resolved and the misalignment when writing subsequent phase etch levels are at most 35 nm.

Test patterns for metrology are shown in Figure 10. The scatterometry patterns are for monitoring variations across the field and the wafer. Test patterns for MEEF are also included.

A set of patterns for double exposure of resists is shown in Figure 11. The large area can be overlaid to program image degradation in order to study image quality issues in developing resist models and in characterizing line-edge roughness. Double exposure of the horizontal and vertical features can be used to create sharp corners for evaluating resist diffusion.

Figure 12 shows monitors for plasma etching surrounded by fields of various feature types and duty cycles that are designed to measure the level of plasma etching effects and the range over which they occur.

Finally, Figure 13 shows CMP test patterns. Note the line orientation effects at the right of the picture as well as the serpentine arrays.

6. CONCLUSIONS

In order to enable the next generation of integrated circuit technology, it is important to find an efficient way of linking residual processing effects back to the circuit design stage. This Design For Manufacturability can be done by searching for patterns in the layout that correspond to certain geometries represented by these effects. The extent to which residual process effects are important and are computationally tractable has yet to be determined. The test patterns in this multi-student test mask are intended to be used in experiments to make these assessments. Experience with a prototype pattern-matching software tool for predicting residual aberration effects is being used to identify important characteristics necessary in an approach based on maximal lateral impact functions and pattern matching.

ACKNOWLEDGEMENTS

This paper was supported by industry and the State of California in a U.C. Discovery program on Feature Level Compensation and Control. Students in the Lithography Network supported by DARPA and Semiconductor Research Corporation also contributed.

The authors would like to thank the following individuals at Photronics for their assistance in the fabrication and metrology of this test mask: Bryan Kasprowicz, Eric Poortinga, Joshua McCord, Marc Cangemi, and James Unruh.

REFERENCES

1. A. Neureuther, F. Gennari, "No-Fault Assurance: Linking Fast Process CAD and EDA," *Proc. SPIE* Vol. **4889**, 10/02.
2. F. Gennari, G. Robins, and A. Neureuther, "Validation of the Aberration Pattern-Matching OPC Process," *Proc. SPIE* Vol. **4692B**, 3/02.
3. L. Liebmann, B. Grenon, M. Lavin, S. Schomody, T. Zell, "Optical Proximity Correction, a First Look at Manufacturability," *Proc. SPIE* Vol. **2322**, 1994.
4. Y. Granik, "Correction for etch proximity: new models and applications," *Proc SPIE* Vol. **4246**, pp. 98-112, 2001.
5. The Windows GDS Viewer by Frank Gennari is available at the UCB LAVA website: http://cuervo.eecs.berkeley.edu/Volcano/
6. G. Robins, K. Adam, A.R. Neureuther, "Measuring Optical Image Aberrations with Pattern and Probe Based Targets", *JVST B*, Vol. **20**, No. 1, pp. 338-343, Feb 2002.
7. G. McIntyre and A. Neureuther, "Characterizing Illumination Angular Uniformity with Phase Shifting Masks," *Proc. SPIE* Vol. **5040**, pp. 162-170, 2003.
8. G. McIntyre and A. Neureuther, "Linear Phase Ring Illumination Monitor," *J. Vac. Sci. Technol.*, Nov/Dec, 2003 (accepted for publication).
9. G. McIntyre and A. Neureuther, "Interferometric-Probe Monitors for Self-Diagnostics of Phase-Shifting Mask Performance." *Proc. SPIE* Vol. **5130**, 2003 (accepted for publication).

FIGURES

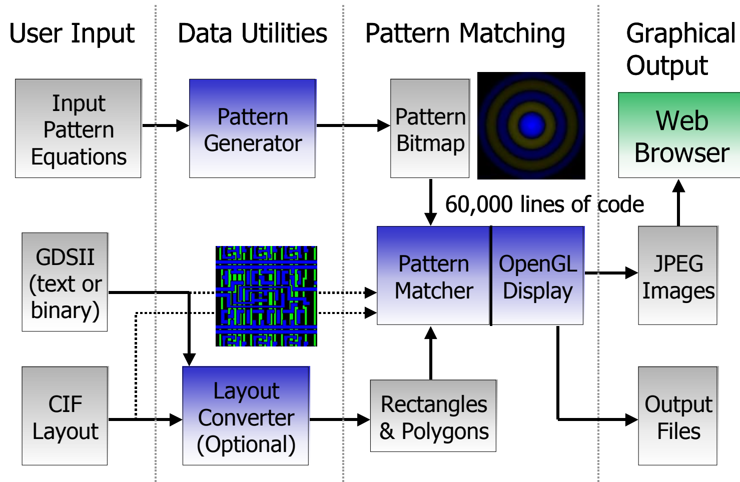

Figure 1: Block diagram of a pattern-matching based system that inspects for worst-case locations of effects of aberrations on a layout[1].

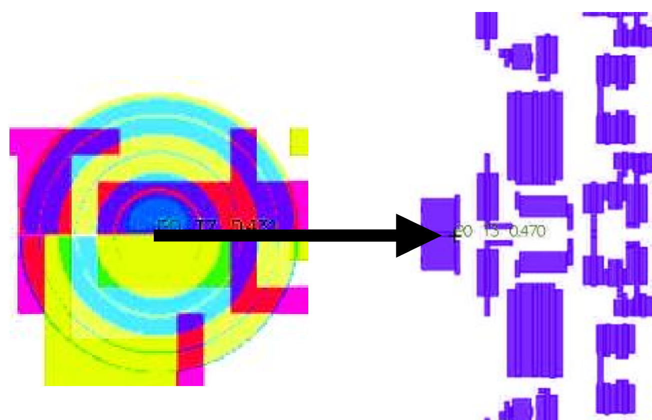

Figure 2: Example of a pattern match for coma and inspection results for a 417mm^2 chip in 0.18µm technology.

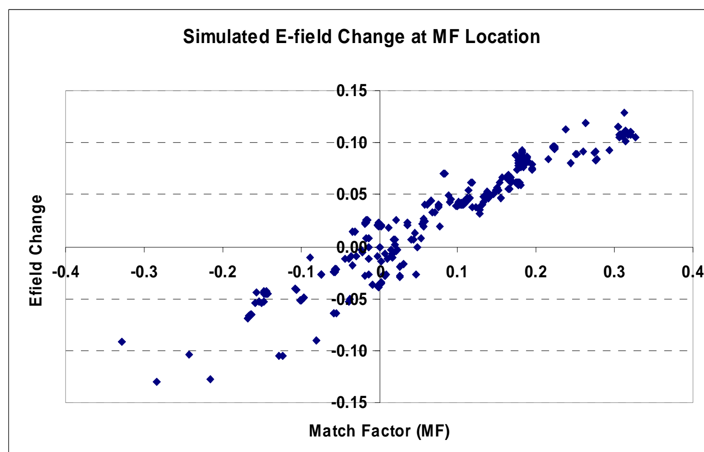

Figure 3: Plot of the intensity change versus match factor for a variety of locations in a layout.

Figure 4: Full view of the multi-student test mask. (I remember seeing this PPT file around)

Figure 5: Floor plan of the test mask.

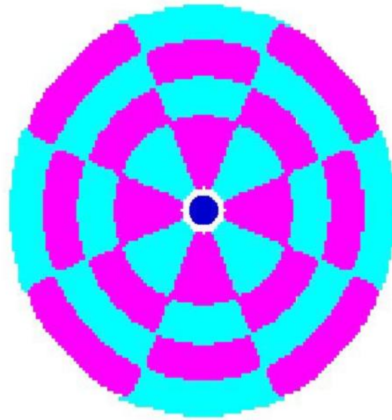

Figure 6: Trifoil aberration monitor and isolated probes used for calibration.

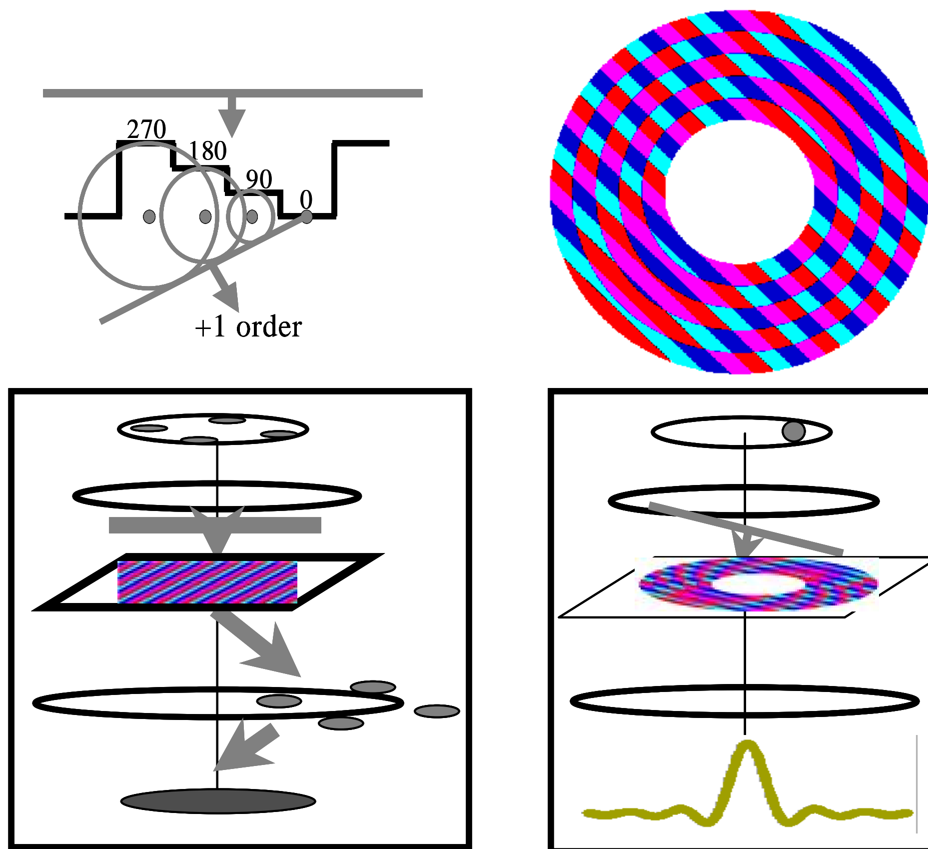

Figure 7: Linear phase grating and linear phase ring illumination monitors.

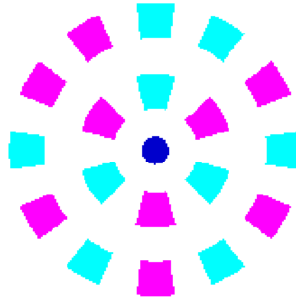

Figure 8: Pattern for testing the error in the depth of the etch in small features.

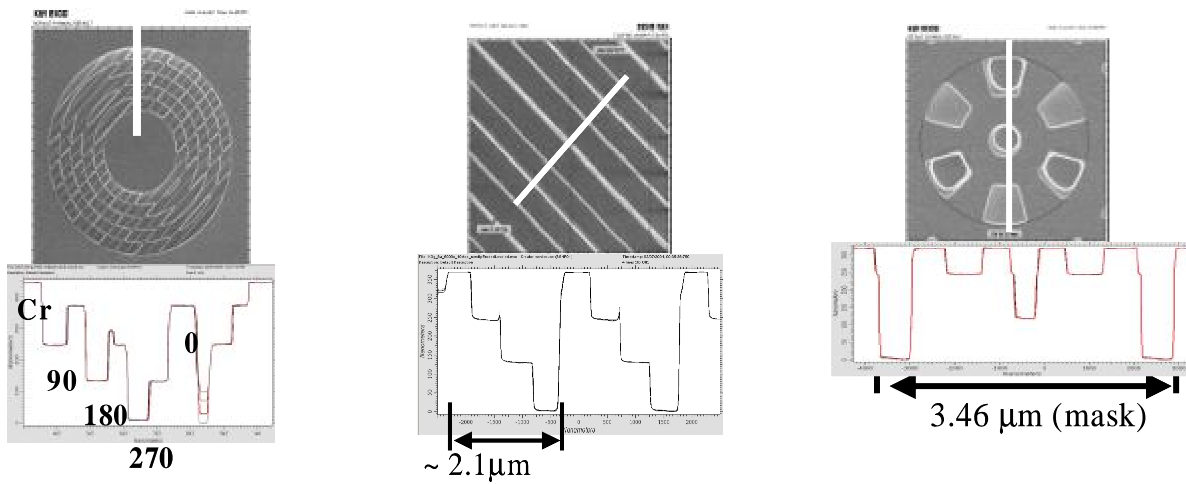

Figure 9: SEMs of mask show high quality mask making.

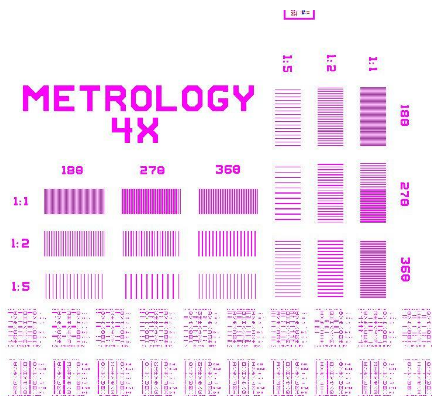

Figure 10: Scatterometry and MEEF test structures.

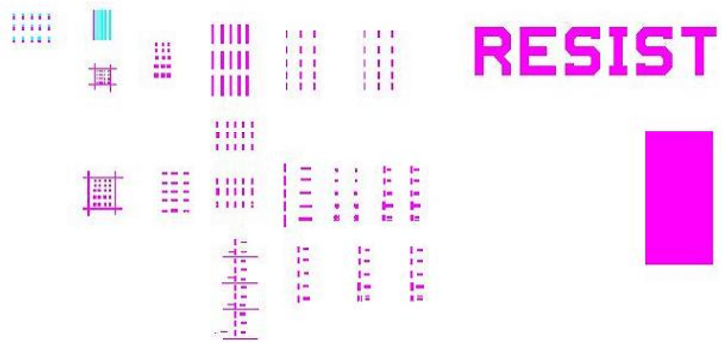

Figure 11: Patterns used for double exposure of resists.

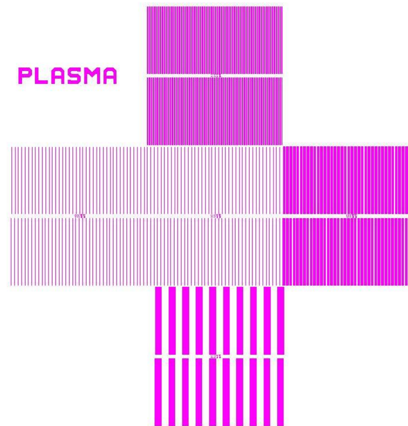

Figure 12: Plasma etch test patterns.

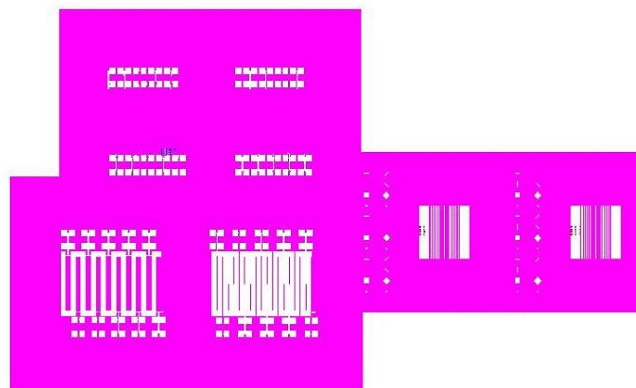

Figure 13: CMP test patterns.