Modeling Within-Die Spatial Correlation Effects for Process-Design Co-Optimization

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Abstract

Within-die spatial correlation of device parameter values caused by manufacturing variations [1] has a significant impact on circuit performance. Based on experimental and simulation results, we (1) characterize the spatial correlation of gate length over a full-field range of horizontal and vertical separation; (2) develop a rudimentary spatial correlation model; and (3) investigate its impact on the variability of circuit performance.

1. Introduction

The aggressive scaling of silicon technology has enabled dramatic improvements in integrated circuit performance. However, as nominal device parameter values are rapidly reduced, control of semiconductor manufacturing processes has become increasingly difficult and expensive. In fact, the 2003 edition of the International Technology Roadmap for Semiconductors [2] lists the control of printed transistor gate length in the lithography process as falling short of expectations; no known manufacturable solution is capable of achieving the target variation value. As variability in manufacturing processes has grown more severe, variations in device parameter values have grown in proportion to nominal values. In turn, wider distributions for device parameters have lead to increased variability in circuit performance, causing worsened yield degradation in successive technology generations. Therefore, the robustness of circuits has emerged as a roadblock (in addition to the problem of increasing power consumption) in modern IC design [1, 3].

In order to combat the growing negative impact of manufacturing variations on circuit performance, two approaches are being taken. The first approach is to apply a renewed focus on process control from a manufacturing perspective, in an effort to directly reduce the variations in device parameters; in the lithography process, for example, the development of integrated, scatterometry-based metrology [4] promises to improve gate CD control. The second approach comes from the design perspective, where practices can be developed to decrease circuit sensitivity to process variation. The most deleterious sources of device parameter variation may be identified through simulation; then, design styles that exhibit special robustness to those sources of variation can be selected.

In both approaches, there is great value in having a complete understanding of the underlying mechanisms that dictate how process variation affects circuit performance. This paper investigates one particular piece of the process-design space—spatial correlation. This is defined as the degree to which the distributions of device parameter (in this case, gate length) values of neighboring, near-neighboring, and well-separated devices are related to each other (as a function of physical separation). As we show in this work, spatial correlation is ultimately a significant factor in circuit performance variability, and a potential point of entry for designing more robust circuits.

2. Empirical modeling of spatial correlation

In order to investigate the impact of spatial correlation on circuit performance, one must first investigate the nature of spatial correlation itself. To this end, this work focuses on the gate length for close spatial correlation analysis, since this parameter is one of the major culprits of process variation [5] and has shown some systematic patterns of variations due to lithography [6]. In three steps, gate length measurements were collected, spatial correlation characteristics were extracted, and a simple model was constructed to capture the general behavior of correlation for the purposes of circuit simulation.

2.1. Gate length measurement

Exhaustive critical dimension (CD) measurements were performed using electrical linewidth metrology (ELM) on a full 200mm wafer processed through an industrial 130nm manufacturing process [7]. The

linewidth of a poly-silicon "gate" is measured via ELM by passing a precisely calibrated current through the gate and measuring the voltage across a subsection of the gate, as shown in **Fig. 1**.

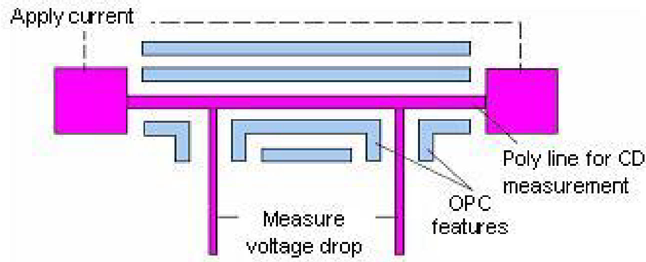


Figure 1. Kelvin test structure for ELM measurement. The measured voltage drop, combined with sheet resistance measurements from neighboring Van der Pauw structures can be used to extract linewidth.

The electrical measurement yields a numerical value with a sizable (~40nm) negative offset from values measured using more standard metrologies such as CDSEM or scatterometry, but the ELM measurements have been shown to have comparable precision to other metrologies and exceptional speed. Due to this speed of measurement, huge quantities of data may be taken—for example, this work makes use of 280 measurements per die over 35 dice, a total of roughly 10,000 measurements (**Fig. 2**). From this full-wafer dataset, the average die CD fingerprint may be extracted (**Fig. 3**) and modeled fairly well using a second-degree polynomial with coefficients calculated by least squares regression (**Fig. 4**). It is clear from this analysis that there exists a strong systematic within-die variation component, due to a combination of mask errors and systematic variation in the exposure tool.

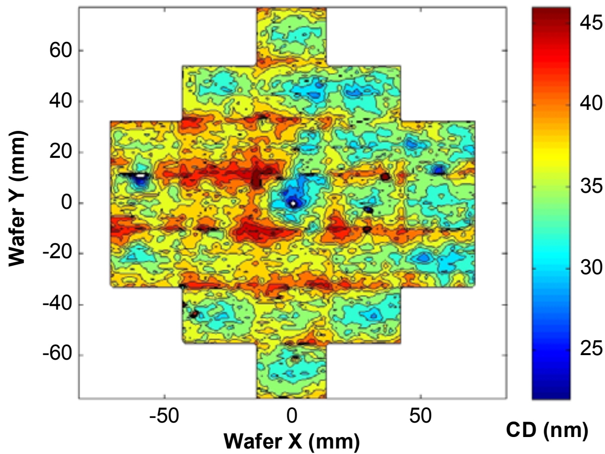


Figure 2. Full-wafer CD measurements.

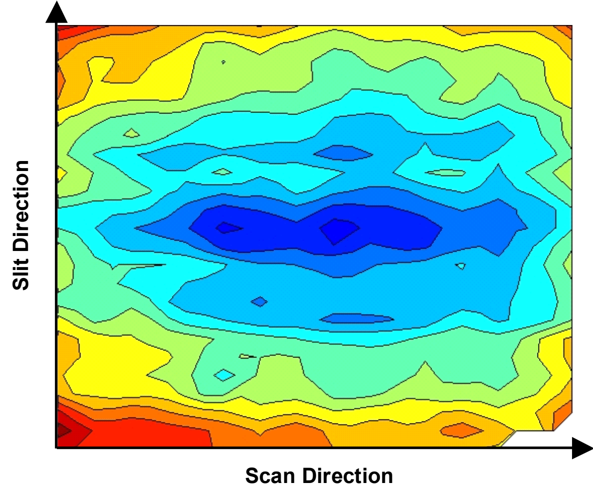


Figure 3. Average within-die CD fingerprint.

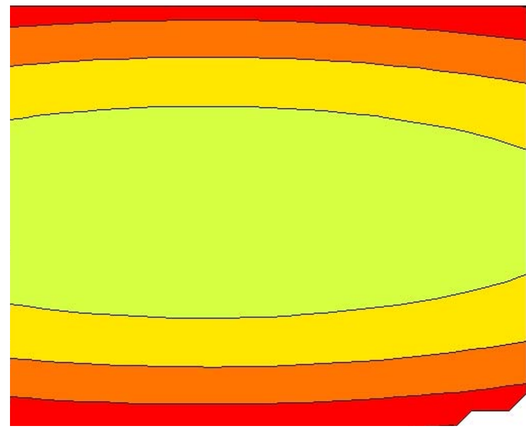


Figure 4. Polynomial model of within-field variation. Cross-sections of this model dictate the nature of horizontal and vertical spatial correlation.

2.2. Spatial correlation characteristics

To extract the spatial correlation characteristics for this lithography process, the CD measurements are standardized against the entire wafer-wide CD distribution using the relation

$$z_i = \left(x_i - \hat{\mu}\right)/\hat{\sigma}\,, \tag{1}$$

where x_i is the ith CD measurement and $\hat{\mu}$ and $\hat{\sigma}$ are the average and standard deviation of all CD measurements. Next, the spatial correlation can be estimated and plotted as a function of separation distance using

$$\rho_{jk} = \left(\sum z_j * z_k\right)/n\,. \tag{2}$$

That is, for each separation distance l afforded by the density of measurements, all pairs of points (j, k) separated by l that fall within the same die are included in the summation as dictated by Eq. 2. Resulting spatial correlation plots for this data set are shown in **Fig. 5** (displaying correlation versus separation measured in the horizontal direction) and **Fig. 6** (displaying correlation versus separation measured in the vertical direction). In both cases, devices separated by relatively short distances have the highest correlation ρ; as the separation increases, ρ falls roughly linearly, then finds a minimum value, and finally begins to increase as the distance approaches the entire width (or length) of the die. It is clear from inspecting the within-die systematic variation fingerprint (shown in **Figs. 3** and **4**) that the increase in correlation at near-field-width separation distances is an artifact of this component of variation. That is, it is easy to see that gate length values at opposite ends of the die are closely related due to the bowl-shaped pattern of the average within die variation. While it is expected that this within-die variation fingerprint is not atypical, we will ignore, for the time being, this upswing-portion of the correlation plot, because we can assume that critical path lengths will rarely exceed roughly half the chip width.

2.3. Spatial correlation model

A simple piecewise linear model (again, ignoring values of separation greater than half the width of the field) was imposed to formally capture the spatial correlation relationship. Illustrated in **Figs. 5** and **6**, the model contains two parameters: X_L, a characteristic correlation length, and ρ_B, the characteristic correlation baseline. By definition, this model approximates the value of spatial correlation (ρ) given the separation distance (x or y) by:

$$\rho = \begin{cases} 1 - \dfrac{x}{X_L}(1-\rho_B), x \le X_L \\ \rho_B, x \ge X_L \end{cases} \quad (3)$$

Physically, X_L is related to the gradient of the within-die systematic variation; ρ_B is determined by the relative magnitudes of within-die and die-to-die variation components (the larger the fraction of total variation accounted for by die-to-die variation, the larger ρ_B will be).

These data are taken from a relatively large test chip covering the entire lithographic field (28 by 22 mm). However, the general shape of the spatial correlation curve will scale along with field size (since the polynomial model of systematic variation is a property of the exposure tool) and is therefore independent of field size. Thus, barring any specific tailoring of the within-die and across-wafer components of variation, and assuming one chip is printed per field, X_L will naturally fall at roughly half the chip length no matter what size field is printed.

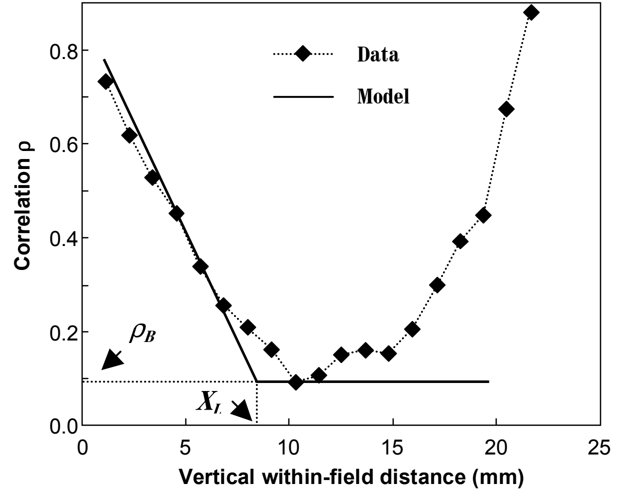


Figure 5. Vertical spatial correlation dependence.

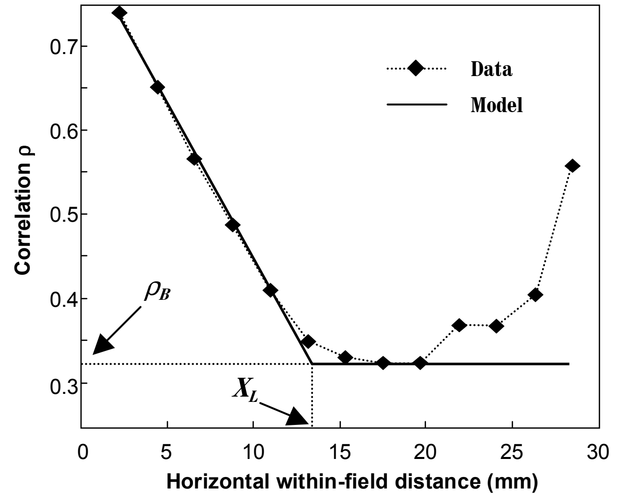


Figure 6. Horizontal spatial correlation dependence.

3. Impact of spatial correlation on circuit performance

It is previously understood that delay variability is aggravated by high spatial correlation. A basic intuition of this effect can be attained through mathematical arguments. Consider the variance of the sum of n identically, normally distributed, correlated random samples:

$$\sigma^2_{tot} = n\sigma_{ind}^2 + 2\rho\left({}_nC_2\right)\sigma_{ind}^2 = \left[n + \rho(n)(n-1)\right]\sigma_{ind}^2 . \quad (4)$$

Using this relationship, we see that when $\rho = 1$, the condition of perfect correlation, $\sigma_{tot} = n\sigma_{ind}$, whereas when $\rho = 0$, the condition of perfect absence of correlation, $\sigma_{tot} = \sqrt{n}\sigma_{ind}$. If we approximate each stage delay in the critical path as a random sample (implicitly assuming that the delay of a given stage depends only on its associated gate length), we see that delay variability will decrease when either X_L or ρ_B is reduced (since this implies a reduction in ρ). This is a fairly accurate approximation—however, the actual impact of spatial correlation on circuit delay variability is slightly weaker (**Fig. 7**) because the assumption of perfect delay independence from one stage to the next is violated.

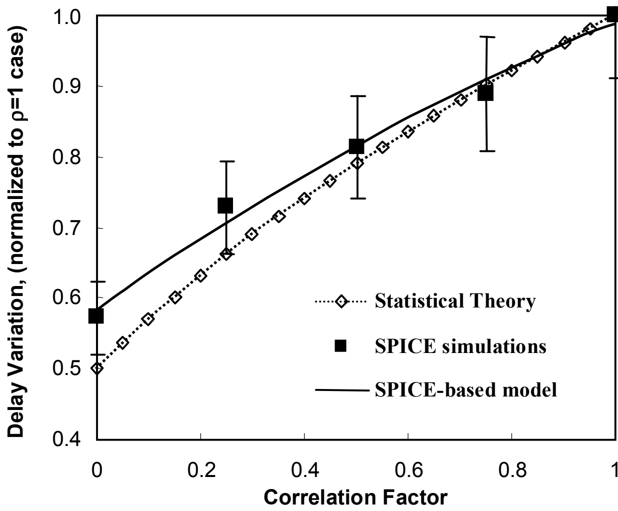
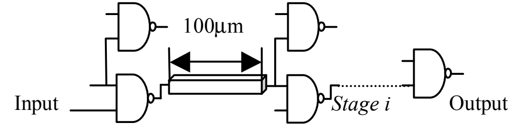


Figure 7. Comparison of statistical theory and SPICE simulation on 4-stage inverter chain.

That is, the discrepancy between mathematical theory and circuit simulation arises because the true delay of a given stage depends not only on its own gate length but also on the gate lengths of the preceding stage (due to input signal transition rate) and following stage (due to capacitive loading).

To compare the improvements in delay variability achieved through the approach of reducing spatial correlation to those possible through the conventional approach of reducing gate length variation, simulations were performed for a canonical critical path subject to variable gate length under different combinations of X_L, ρ_B, and σ_L/μ_L. The canonical circuit (**Fig. 8**) consists of 10 equally-sized NAND stages, each loaded by a fan-out of two and separated from the following stage by 100μm of local interconnect. Nominal device parameter values and variances are based on an industrial 90nm technology node. The Berkeley Predictive Technology Model (BPTM) is employed to project the interconnect parameters and extract RC parasitics [8]. For simulation efficiency, an analytical model of a single stage delay was developed as a function of gate length. The values of model coefficients were extracted from HSPICE simulations (**Fig. 9**).



$$Stage\ Delay\ (ps) = \left[4.91 + 3.52\left(\frac{\Delta L}{L}\right)_i - 2.67\left(\frac{\Delta L}{L}\right)_i^2\right] \cdot \left[4.28 + 0.07\left(\frac{\Delta L}{L}\right)_{i+1} + 0.34\left(\frac{\Delta L}{L}\right)_{i+1}^3 + C_{interconnect}\right]$$

Figure 8. Canonical critical path circuit (10-stage NAND chain, Fan-Out=2).

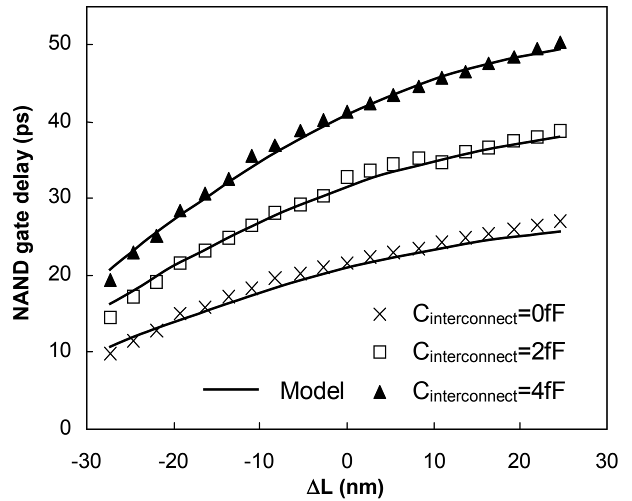


Figure 9. Model verification with SPICE simulations.

Next, this analytical model was used to generate 3000 Monte Carlo simulations under nominal conditions of X_L = 2mm, ρ_B = 0.2, and σ_L/μ_L = 10%. (The value of X_L was intentionally reduced when compared to the values extracted from the 130nm-generation test structures to reflect the smaller chip size as well as potential for reducing X_L directly through process control schemes.) The results, shown in **Fig. 10**, indicate that delay variability is most sensitive to the tuning of σ_L/μ_L; however, reduction of both X_L and ρ_B does display some benefit in terms of reducing delay variability. While the improvement due to direct reduction of parameter variation is linear, the improvement due to reduction of spatial correlation parameter X_L increases gradually as the scaling factor is reduced, achieving over half of the total

potential improvement with the final 25% reduction of X_L. Also notable is the fact that the greatest gains in reducing ρ_B are seen when X_L is also strongly reduced.

These data show that indeed spatial correlation provides us with a significant lever for reducing circuit delay variation. If new process control schemes allow us to tune X_L and ρ_B arbitrarily, we can expect to see up to a *4x* improvement in delay variability. Although this method may be less efficient than reducing process variation directly, that strategy has long been a well-known manufacturing goal. Thus, the potential for gains in this area have already planned for on industry roadmaps, whereas spatial correlation concerns are as of yet an untapped resource for robust design.

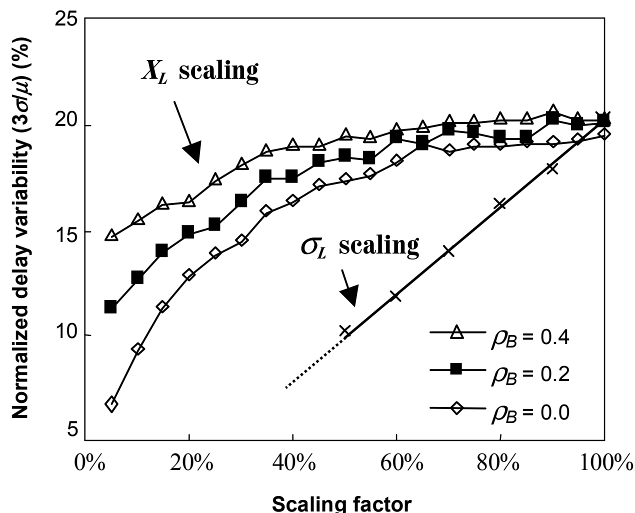


Figure 10. Comparison of impacts of spatial correlation and normalized variation in gate length on critical path delay variability.

Alternatively, we could view these results from a design perspective; reducing X_L is equivalent to increasing the separation between successive stages in a circuit path. In this sense, our results indicate that the optimal design in terms of spatial correlation would situate successive stages with maximum separation, ideally up to a distance X_L apart. While this is currently impractical because X_L is roughly half the die size, this parameter may become tunable in the near future due to adjustments in the exposure step. For example, by using graduated filters to reduce across-slit variation and modulated laser pulse energy to reduce variation along the scan [9], both intra-field variation and spatial correlation can be reduced dramatically, enabling substantial reduction in delay variability. In addition, ρ_B can be reduced by minimizing the fraction of total variability accounted for by die-to-die variation. The wisest approach for leveraging our understanding of the effects of spatial correlation in critical path optimization will be to use process control schemes in manufacturing to tune X_L and ρ_B lower as well as to incorporate circuit design rules to increasing the separation between successive stages to minimize the degree of correlation "seen" by the circuit.

4. Non-Critical Path Elements

As we have shown, minimization of correlation between successive stages in a critical path is the optimal design strategy for minimizing the path delay variability due to spatial correlation. However, there are a number of situations in which spatial correlation may actually improve circuit performance. Specifically, in circuit elements whose performance depends on the matching of two or several critical components, high local spatial correlation is beneficial. These types of circuits include many analog applications, such as amplifiers, as well as memory elements, such as SRAM cells.

Therefore, since circuit elements exist that require accurate matching, reasonable correlation levels should be targeted based on system-level design considerations.

5. Conclusion

A simple analytical model for spatial correlation is derived from experimental CD measurement data. Based on this model, we find that in order to minimize critical path delay variability, the process should be tuned to reduce X_L and ρ_B, and the critical path should be designed to space stages apart by a large distance (up to X_L).

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